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(54) Electrical device comprising a voltage dependant capacitance and method of manufacturing the same

(57) An electrical device 10 having a voltage dependent capacitance is provided comprising a first region 12 of a semiconductor material, and a second region 13 and a third region 14 of a semiconductor material formed in the first region, the second and third regions being separated by a separation region, and an electrically insulating layer 15 formed on the first region at least at a region corresponding to the separation region, and a substantially conductive element 16 formed on the insulating layer at least at a region corresponding to the separation region such that the insulating layer electrically insulates the substantially conductive element from the first, second and third regions, and a first electrode 17 connected to the substantially conductive element, and a second electrode 18 connected to the second and third regions. A method of manufacturing the device is also disclosed.

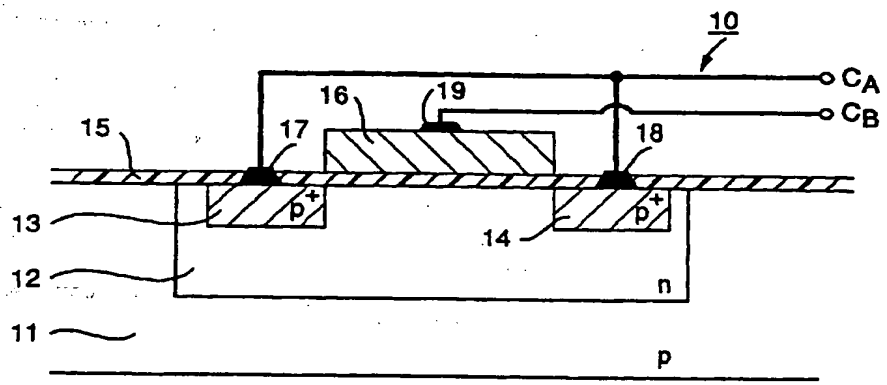

Fig. 1

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for a DC de-coupling capacitor.

[0010] The present invention also provides a VCO, a PLL and a radio communication device making use of a varactor as discussed above. Furthermore, a method of manufacturing a varactor according to the present invention is provided.

[0011] An advantage of the present invention is that a varactor having a high quality factor, Q, *i.e.* with low series resistance, may be realised even for high frequency applications by using a conventional CMOS process without adding any manufacturing steps. The varactors may therefore be manufactured at high yield and to low costs.

[0012] Furthermore, an advantage of the present invention is that a VCO is provided which may be realised by using a conventional CMOS process and which does not need a DC de-coupling capacitor in the design. This makes the implementation of the VCO inexpensive and physically small since no DC de-coupling capacitor is needed neither on the IC nor externally to the IC on a PCB. These advantages becomes even more pronounced when implemented in hand-held devices, such as portable phones, which need to be small and which are produced in high-volumes.

[0013] Advantageously, the present invention provides an integrated Voltage Controlled Oscillator and/or Phase Locked Loop, PLL, circuit, which include a varactor as discussed above, by using a conventional CMOS process.

[0014] Since many of the functions of a radio communication device may be integrated by conventional CMOS processes, the integration of a VCO and/or a PLL circuits together with these functions allows the present invention to provide a radio communication device with a high degree of integration and thus small physical dimensions. The high degree of integration also reduces the manufacturing costs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

FIG 1 illustrates a varactor according to a first embodiment of the present invention comprising a PMOS enhancement transistor;

FIG 2 illustrates a varactor according to a second embodiment of the present invention comprising a NMOS enhancement transistor;

FIG 3 illustrates a varactor according to a third embodiment of the present invention comprising a NMOS depletion transistor;

FIG 4 illustrates an operational aspect of the first embodiment of the present invention;

FIG 5 illustrates an equivalent circuit diagram of the first embodiment of the present invention;

FIG 6 illustrates a circuit diagram of a Voltage Controlled Oscillator according to a fourth embodiment of the present invention;

FIG 7 illustrates a top-view of a composite varactor according to a fifth embodiment of the present invention;

FIG 8 illustrates a cross-section view along the axis VIII-VIII of FIG 7;

FIG 9 illustrates a cross-section view along the axis IX-IX of FIG 7;

FIG 10 illustrates a top-view of a composite varactor according to a sixth embodiment of the present invention;

FIG 11 illustrates a cross-section view along the axis XI-XI of FIG 10;

FIG 12 illustrates a cross-section view along the axis XII-XII of FIG 10;

FIG 13 illustrates a cross-section view along th axis XIII-XIII of FIG 10.

DETAILED DESCRIPTION OF EMBODIMENTS

[0016] Embodiments of the present invention ar described below, by way of example only. It should b noted that details illustrated in the figures may not b drawn to scale. On the contrary, the dimensions of the details of the illustrations are chosen so as to improve the understanding of the present invention.

[0017] According to the present invention there is provided an electrical device having a voltage dependent capacitance. Such a device is also called a varactor. It will be appreciated that the varactor of the present invention may easily be integrated in a conventional CMOS process.

[0018] FIG 1 illustrates a varactor 10 according to a first embodiment of the present invention comprising a PMOS enhancement transistor. The transistor is formed in a p-type silicon substrate 11. An n-type well 12 is formed in the p-type silicon substrate 11 from a first principal surface of the substrate and a p^+-type source region 13 and a p^+-type drain region 14 are formed in the n-type well 12. The impurity concentration of the source and drain regions 13, 14 is chosen to be greater than the impurity concentration of the well region 12. Thereafter an insulating layer 15, preferably of silicon oxide, is formed on the first principal surface of the substrate and a poly-silicon gate 16 is formed on the insulating layer 15 at least covering a part of the n-well region 12 separating the source region 13 and the drain region 14 and such that the gate 16 is electrically insulated from the n-well region 12. A common electrode C_A of the varactor 10 is formed by connecting the source region 13 to the drain region 14. Connection is made to the source region 13 and the drain region 14 by means of a source electrode 17 and a drain electrode 18, respectively. A second electrode C_B of the varactor 10 is connected to the gate 16 by means of a gate electrode 19.

[0019] FIG 2 illustrates a varactor 20 according to a second embodiment of the present invention comprising a NMOS enhancement transistor. The transistor is

actor having a capacitance with a sometimes unacceptable small numerical value. This problem is solved by connecting a suitable number of varactors in parallel to form a composite varactor. The connections between the varactors are preferably carried out by means of a low resistance material, such as aluminium, to keep the resistance between the devices low and thereby achieving an overall high Q factor of the composite varactor.

[0025] As mentioned above, the depletion layer capacitance C_D is also dependent on the potential of the well and, consequently, the device may also be operated by applying fixed potentials to the electrodes C_A and C_B and controlling the capacitance of the device by a suitable voltage applied to the well. Alternatively, a fixed potential is applied to one of the electrodes C_A or C_B, the other electrode is connected to the well and the device is controlled by a suitable voltage applied to the well.

[0026] The operational aspects of the first embodiment discussed above applies also to the second and third embodiments after appropriate adaptations to the applied polarities according to principles well known in the art.

[0027] Although the first, second and third embodiments discussed above all makes use of a p-type semiconductor substrate, n-type semiconductor substrate may be used equally well if polarities and conductivity-types are adapted according to well known principles in the art.

[0028] In a conventional 0.25μm or 0.35μm CMOS process the gate length L_g, corresponding substantially to the distance between the source region and the drain region, is preferably chosen to be less than 2μm and most preferably less than 1μm. The gate width W_g is preferably chosen to be less than 20μm, *e.g.* 15μm, 10μm or 5μm. In the case where a low resistance gate material, such as metal silicided poly-silicon, is used the gate width may be chosen to be less than 6μm.

[0029] FIG 6 illustrates a circuit diagram of a Voltage Controlled Oscillator 60 according to a fourth embodiment of the present invention. The bulks and the sources of a first, a second and a third NMOS enhancement transistor, T_1, T_2, and T_3, respectively, are connected to ground potential. The gate of the first transistor T_1 is connected to the drain of the second transistor T_2 and to the gate of the third transistor T_3. The gate of the second transistor T_2 is connected to the drain of the first transistor T_1 and to a first electrode of first inductor L_1. A second electrode of the first inductor L_1 is connected to a first electrode of a first resistor R_1.

[0030] The drain of the second transistor T_2 is connected to a first electrode of a second inductor L_2. A second electrode of the second inductor is connected to a second resistor R_2. A second electrode of the first resistor R_1 is connected to a second electrode of the second resistor R_2 to a first electrode of a third resistor R_{ext} and to a first electrode of a first capacitor C_{ext}. A second electrode of the third resistor R_{ext} is connected to a supply voltage $+V_{cc}$ and a second electrode of the first capacitor C_{ext} is connected to ground potential. The circuit further comprises at least two varactors V_1-V_n where n is the number of varactors. A first composite varactor is formed by coupling a predetermined number of the varactors V_1-V_n in parallel and a second composite varactor is formed by connecting the remaining varactors in parallel. An input connection for receiving a voltage V_{freq} which controls the frequency of the Voltage Controlled Oscillator is connected to a first electrode of each of the first and second composite varactors. A second electrode of the first composite varactor is connected to the drain of the first transistor T_1 and a second electrode of the second composite varactor is connected to the drain of the second transistor T_2. In this embodiment, the varactors V_1-V_n are made up of NMOS depletion transistors. The first electrodes of the composite varactors is constituted by a common connection between the bulk and all the source regions and drain regions of the NMOS depletion transistors. The second electrode of the first composite varactor is constituted by a common connection between the gates of the NMOS depletion transistors of the first composite varactor and the second electrode of the second composite varactor is constituted by a common connection between the gates of the NMOS depletion transistors of the second composite varactor. The gates of the NMOS depletion transistors are preferably connected to the VCO circuit, and not to the input connection for receiving a voltage V_{freq}, since the gate has a low parasitic capacitance. The output signal I_{out} of the VCO is obtained at the drain of the third transistor T_3. Optionally the third resistor R_{ext} and the first capacitor C_{ext} are not integrated on the chip. Furthermore, it is possible to implement the first and second inductors L_1, L_2 by making use of the inductance of bonding wires of the IC. It should be noted that the bulk of the MOS transistors making up the composite varactors V_1-V_n may be connected to a different potential than V_{freq}, *e.g.* zero potential, as long as the bulk does not form a forward biased diode with any other regions of the transistors. The operation of the VCO circuit, as such, is well known in the art.

[0031] The best performance for a given VCO circuit with given inductors is determined by the Q factor and the dynamic range (minimum and maximum capacitance value) of the (composite) varactors. According to the fourth embodiment of the present invention NMOS transistors are used. These gives the lowest parasitic resistance and thus the highest Q factor. The threshold voltage is adjusted such as to give the largest dynamic range of the (composite) varactors as is possible within a pre-determined (voltage) bias range.

[0032] In the case where the varactors of the present invention are integrated in a conventional CMOS process together with other devices the source and drain regions need to be insulated from the substrate, for example by forming the varactor in at least one well

that one common gate 86 is formed. The gate 86 forms a first electrode of the composite varactor 80 and the p^+-type region 83, 91, 84, 90 is connected to a second electrode (not shown) of the composite varactor 80.

[0039] In an example of a method of manufacturing the composite varactor 80 of the sixth embodiment the n-type well region 82 is formed in the p-type semiconductor substrate 81. An insulating layer (not shown) is formed on the surface of the well region and a poly-silicon layer is formed thereon. A first mask layer (not shown) is formed on the poly-silicon layer. The first mask layer is exposed and etched to form a first mask (not shown) having a comb-shaped form. Next, the poly-silicon layer is etched to form the gate 86. The gate 86 consequently adopts the comb-shaped form of the mask. The gate 86 forms a first electrode of the composite varactor. The remainder of the mask is removed and a second mask layer (not shown) is formed on the structure. The second mask layer is exposed and etched to form a second mask (not shown) with an opening such that the "fingers" of the comb-shaped gate and an area surrounding the "fingers" are not covered by the mask. Thereafter, a p^+-type source region 83, combined p^+-type source and drain regions 91, a drain region 84 and connection regions 90 for connecting these regions are formed by ion-implantation using not only the second mask but also the gate 86 as a mask. During this process the conductivity of the gate 86 will increase due to the ion-implantation of the gate. Alternatively, the first mask is kept during the ion-implantation. Preferably, the conductivity of the gate is increase by having the gate 86 metal silicided. The ion-implanted regions 83, 91, 84 and 90 are connected and this connection forms a second electrode of the composite varactor.

[0040] The device of the sixth embodiment can be considered as made up of a number of MOS transistors, each having a source region 91 (or 83), a drain region 91 (or 84) a gate 86 and a channel region formed between the source region and the drain region, which are coupled in parallel by means of the connection regions 90 to form a composite varactor. The operation of each of the MOS transistors will therefore correspond to the operation of the varactors comprising a MOS transistor as discussed above. In an alternative embodiment (not shown) the gate 86 is formed (at least temporary during the manufacturing) such that it also performs the function of the second mask and, hence, no second mask is needed to define the regions which are to be ion-implanted 83, 91, 84 and 90 in the steps that follow.

[0041] The composite varactors (70, 80) of the fifth and sixth embodiments show examples of devices having a number of varactors coupled in parallel. As discussed above, a high Q factor of each varactor can be achieved by using small dimensions of the gate and the channel region and by keeping the resistance of the gate (and its connection) as small as possible. Small dimensions of the gate and the channel region do, however, give rise to a varactor having a capacitance with a sometimes unacceptable small numerical value. A suitable capacitance of a composite varactor, *e.g.* the composite varactors of the fifth and sixth embodiments (70, 80), is therefore achieved by coupling a suitable number of varactors in parallel. Composite varactors having high Q factors and suitable capacitances are thereby provided.

[0042] It should be noted that although the devices of the fifth and sixth embodiments have been illustrated by means of their method of manufacturing, other methods of manufacturing which may be contemplated by the man skilled in the art may be used without departing from the scope of the present invention. Furthermore, it is obvious that a device with any number of MOS transistors coupled together may be formed.

[0043] An advantage of the present invention is that varactor having high quality factors, Q, *i.e.* with low series resistance, may be realised even for high frequency applications by using a conventional CMOS process without adding any manufacturing steps. The varactors may therefore be manufactured at high yield and to low costs.

[0044] Furthermore, an advantage of the present invention is that a VCO is provided which may be realised by using a conventional CMOS process and which does not need the addition of a DC de-coupling capacitor to the design. This makes the implementation of the VCO inexpensive and physically small since no DC de-coupling capacitor is needed neither on the IC nor externally to the IC on the PCB. These advantages becomes even more pronounced when implemented in hand-held devices, such as portable phones, which need to be small and which are produced in high-volumes.

Claims

1. An electrical device (10; 20; 30; 40; V_1-V_n; 70; 80) having a voltage dependent capacitance comprising:

   a first region (12; 22; 32; 72; 82) of a semiconductor material; and
   a second region (13; 23; 33; 73; 83, 91) and a third region (14; 24; 34; 74; 84, 91) of a semiconductor material formed in the first region, the second and third regions being separated by a separation region; and
   an electrically insulating layer (15; 25; 35) formed on the first region at least at a region corresponding to the separation region; and
   a substantially conductive element (16; 26; 36; 76; 86) formed on the insulating layer at least at a region corresponding to the separation region such that the insulating layer electrically insulates the substantially conductive element from the first, second and third regions; and
   a first electrode (17; 27; 37) connected to the

23. A Phase Locked Loop circuit comprising a varactor according to any one of claim 1 to claim 14.

24. A Phase Locked Loop circuit comprising a Voltage Controlled Oscillator according to any one of claim 15 to claim 22.

25. A radio communication device comprising a Voltage Controlled Oscillator according to any one of claim 15 to claim 22.

26. A radio communication device comprising a Phase Locked Loop circuit according to any one of claim 23 to claim 24.

27. A method of manufacturing an electrical device having a voltage dependent capacitance comprising the steps Of:

forming a first semiconductor region; and
forming a second region and a third region of a semiconductor material in the first region, the second and third regions being separated by a separation region; and
forming an electrically insulating layer on the first region at least at a region corresponding to the separation region; and
forming a substantially conductive element on the insulating layer at least at a region corresponding to the separation region such that the insulating layer electrically insulates the substantially conductive element from the first, second and third regions; and
forming a first electrode electrically connected to the substantially conductive element; and
forming a second electrode electrically connected to the second and third regions.

28. A method of manufacturing an electrical device according to claim 27 further comprising the steps of:

forming a blocking layer, for blocking a later MIS transistor threshold implantation step of an IC manufacturing process, at least at a region corresponding to the separation region.

29. A method of manufacturing an electrical device according to claim 28 wherein the IC manufacturing process is a CMOS process.

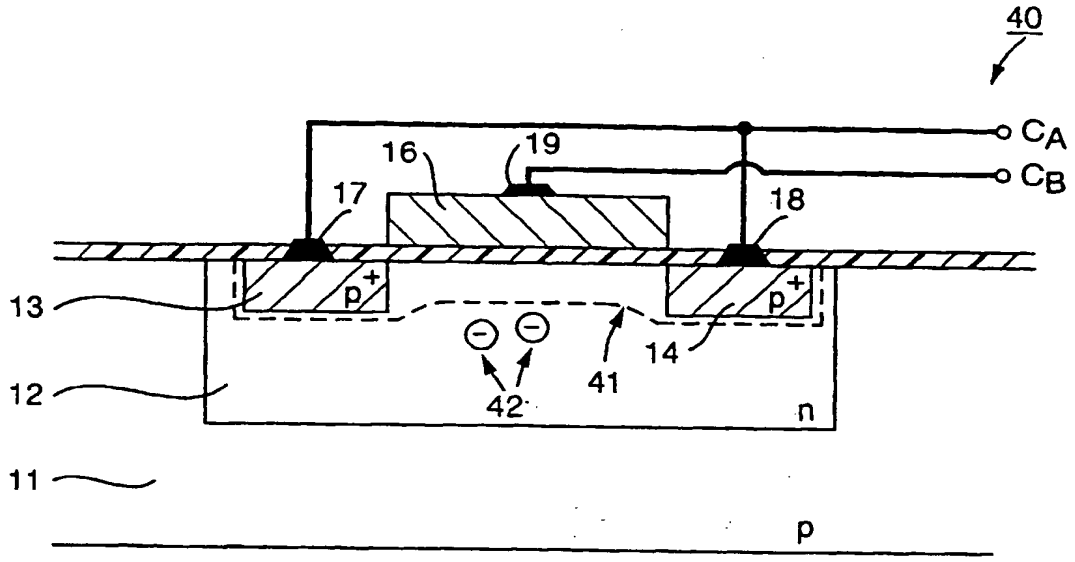

Fig. 4

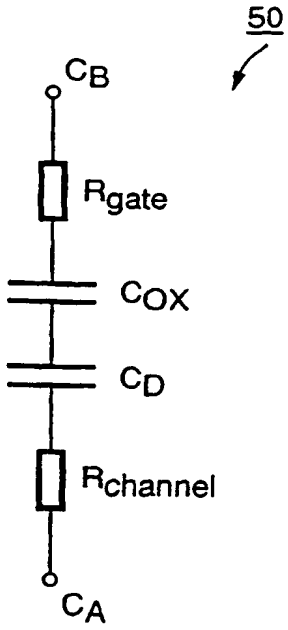

Fig. 5

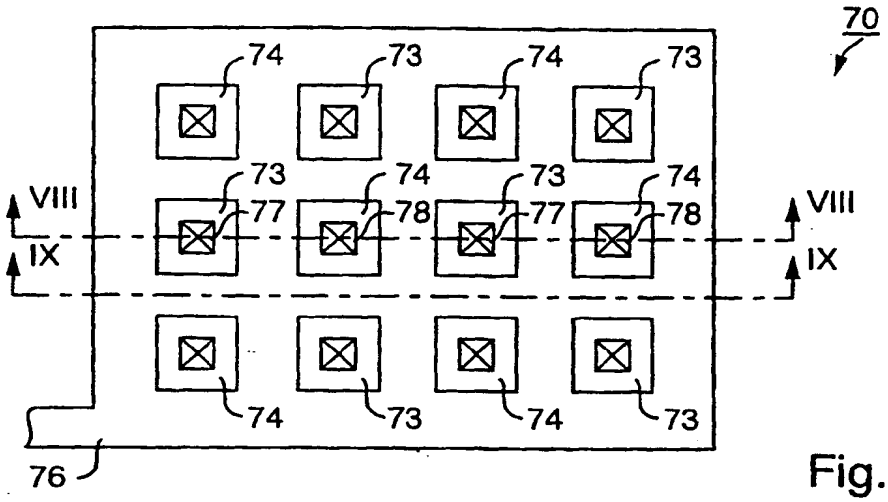

Fig. 7

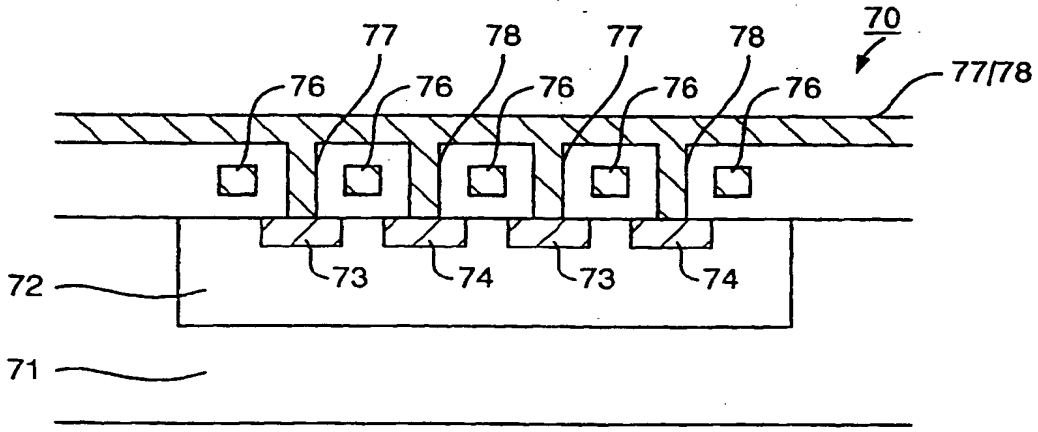

Fig. 8

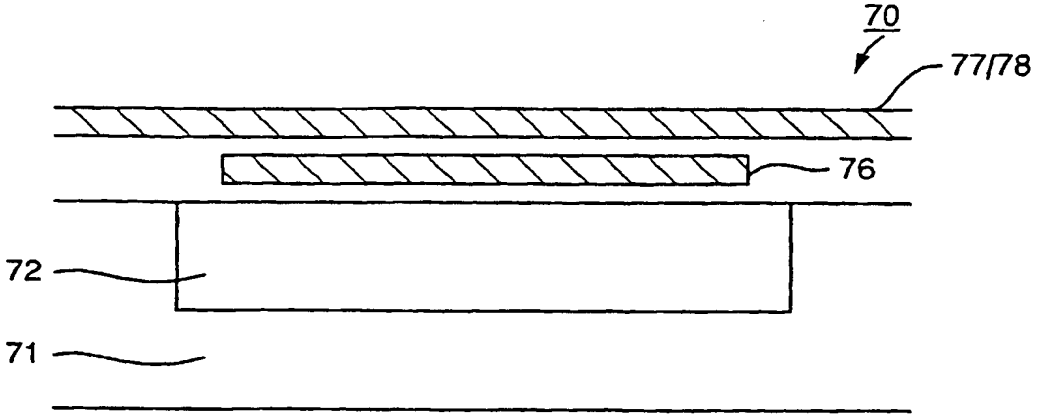

Fig. 9

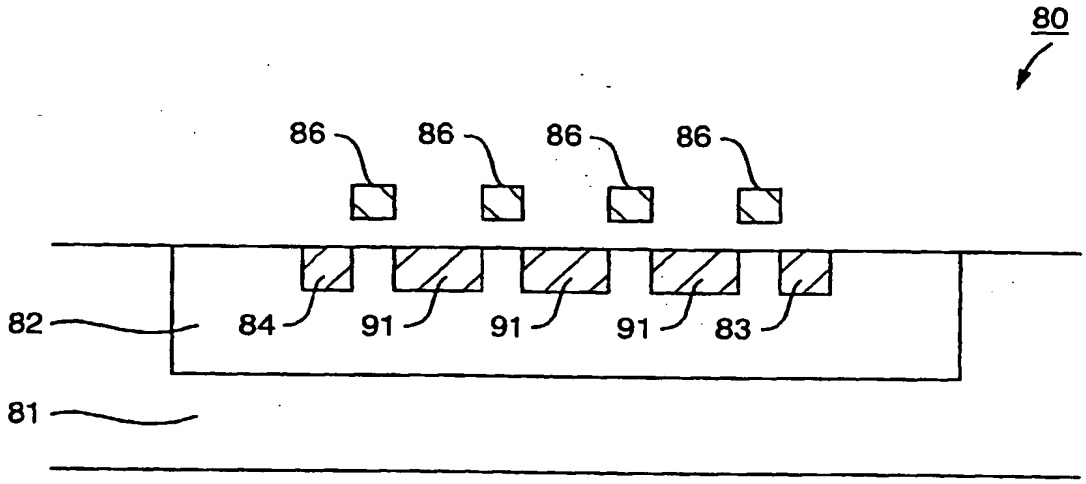

Fig. 13